IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A transistor memory array, comprising:

a first plurality of non-volatile user programmable memory cells, each including a first select transistor and a non-volatile memory transistor including at least one area having a gate oxide layer region disposed near a diffused region with a thickness less than a second gate oxide thickness disposed over a channel region ~~and a first select transistor;~~ and

a second plurality of mask programmed single conductive layer electrode read-only memory cells each including a mask programmed memory transistor and a second select transistor, the non-volatile memory cells and a read-only memory cells having the same footprint within a single memory array.

2. (Cancelled)

3. (Previously Presented) The memory array of claim 1 wherein said footprint has a longitudinal dimension and a width dimension that are the same for both the first and second pluralities of memory cells, with the respective first or second select transistor and memory transistor having a shared electrode in each memory cell.

4. (Previously Presented) The memory array of claim 1 wherein the read-only memory cells include cells having transistors with substrates having open channels and cells having transistors with substrates having shorted channels.

5. (Previously Presented) The memory array of claim 1 wherein the non-volatile memory cells have two poly layers and the read-only memory cells have one poly layer.

6. (Previously Presented) The memory array of claim 1 wherein the second plurality of read-only memory cells is grouped into rows.

7. (Previously Presented) The memory array of claim 6 wherein said group of rows of read only memory cells has a first subgroup of transistors in at least one row in a first logic state.

8. (Previously Presented) The memory array of claim 7 wherein said group of rows of read-only memory cells has a second subgroup of transistors in the at least one row in a second logic state.

9. (Previously Presented) The memory array of claim 4 wherein the channels in the transistors with substrates having open channels and in the transistors with substrates having shorted channels in the read-only memory cells are defined by a buried depletion implant in said substrate, the extent of the implant defining the open and shorted channels.

10. (Previously Presented) The transistor array of claim 1 wherein said non-volatile memory cells have EEPROM transistors.

11. - 19. (Cancelled)

20. (Withdrawn) A transistor memory array comprising:

a plurality of memory cells all having the same areawise footprint including first memory cells having a user programmable EEPROM transistor, second memory cells having a mask programmed read only memory transistor in a first logic state, and third memory cells having a mask programmed read only memory transistor in a second logic state.

21. (Withdrawn) The transistor memory array of claim 20 wherein each memory cell has a select transistor communicating with the memory transistor.

22. (Withdrawn) The transistor memory array of claim 20 wherein said read only memory transistors are in a row.

23. (Withdrawn) The transistor memory array of claim 20 wherein the memory cells having a read only memory transistor in a first logic state have a permanently open channel.

24. (Withdrawn) The transistor memory array of claim 20 wherein the memory cells having a read only memory transistor in a second logic state have a permanently shorted channel.

25. (Withdrawn) A transistor memory array comprising diverse memory cells in a memory array all having the same areawise footprint, a first group of memory cells being user programmable and a second group of memory cells being mask programmed.

26. (Withdrawn) The memory cell of claim 25 wherein said diverse memory cells comprise non-volatile memory transistors and read only memory transistors.

27. (Withdrawn) The memory array of claim 26 wherein said read only memory transistors comprise a first group of transistors in a first logic state and a second group of transistors in a second logic state.

28. (Withdrawn) The memory array of claim 27 wherein each of the memory transistors in said first group is in a first common row and each of the memory transistors in the second group is in a second common row.

29. (Withdrawn) The memory array of claim 25 wherein each memory cell comprises a memory cell and a select transistor.

30. (Withdrawn) The memory array of claim 27 wherein the first group of memory transistors has open channels and the second group of memory transistors has shorted channels.

31. (Previously Presented) The memory array of claim 1 comprising a second plurality of non-volatile user programmable memory cells.